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Title of Invention:	Method and apparatus for defect analysis of semiconductor integrated circuit
First Named Inventor/Applicant Name:	Masahiro Ishida
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		02008071003_rtoa.pdf	120679 e1148e6a7c980aea7d08f6ada63c71287fd4ea59	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Miscellaneous Incoming Letter	1	1
	Amendment After Final	2	2
	Applicant Arguments/Remarks Made in an Amendment	3	5
Warnings:			
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